WE CLAIM:

1. A semiconductor device comprising:

a semiconductor chip having a planar active surface including an integrated circuit protected by an inorganic overcoat, said circuit having metallization patterns including a plurality of contact pads;

each of said contact pads having an added conductive layer on said metallization, said added layer having a conformal surface adjacent said chip, including peripheral portions of said overcoat, and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting.

2. The device according to Claim 1 further comprising:

a non-conductive adhesive layer over said overcoat, filling the spaces between said added conductive layers on each of said contact pads.

3. The device according to Claim 1 further comprising:

a distribution of said contact pads arrayed in the center of said chip in close proximity to the chip neutral line.

4. The device according to Claim 1 wherein said chip metallization is aluminum, copper, or alloys thereof.

5. The device according to Claim 1 wherein said conductive layer consists of at least two conductive sub-layers, one being a conductive diffusion barrier, the other, outer layer being bondable.

6. The device according to Claim 1 wherein said conductive diffusion barrier is selected from a group consisting

of nickel, vanadium, titanium, tungsten, tantalum, osmium, chromium, and aluminum.

7. The device according to Claim 1 wherein said bondable layer is selected from a group consisting of gold, palladium, platinum, silver, and alloys thereof.

8. The device according to Claim 1 wherein said outer surface has a flatness suitable for metal interdiffusion with another flat surface formed by a metal suitable for interdiffusion.

9. The device according to Claim 1 wherein said inorganic overcoat is moisture impermeable and stiff.

10. The device according to Claim 1 further comprising:

a distribution of said contact pads such that an area portion of said active chip surface is available for attaching a thermally conductive plate, said plate having a thickness compatible with the thickness of said conductive pad layer.

11. The device according to Claim 10 wherein said plate has an outer surface suitable for metallurgical bonds.

12. The device according to Claim 10 wherein said plate surface is solderable.

13. The device according to Claim 10 wherein said contact pads are arrayed along the periphery of said chip and said plate is located inside said periphery.

14. The device according to Claim 10 wherein said contact pads are arrayed in the center of said chip and said plate is formed as a frame around said contact pads.

15. The device according to Claim 1 wherein said semiconductor chip is made from a material selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material used in integrated circuit fabrication.

16. The device according to Claim 1 further comprising encapsulation material protecting at least the chip surface opposite said active surface.

17. The device according to Claim 16 wherein said encapsulation material is a molding compound.

18. The device according to Claim 1 further comprising a metallic or insulating substrate having terminal pads aligned with the distribution of said chip contact pads, each terminal pad being bonded to one of said chip contact pads having said added layer, respectively, such that electrical contact between said chip and said substrate is established, while forming a gap therebetween having a width of approximately said added layer thickness.

19. The bonding according to Claim 18 wherein said bonding is selected from a group of techniques and materials comprising:

direct welding by metallic interdiffusion;

attachment by solder paste; and

attachment by conductive adhesive.

20. The device according to Claim 18 further comprising encapsulation material protecting at least the chip surface opposite said active surface and filling said gaps.

21. The device according to Claim 18 further comprising a substrate addition suitable for attaching said device to a board, said addition selected from a group consisting of solder balls, conductive lands, and bondable surface finish.

22. The device according to Claim 1 further comprising a protective layer on the chip surface opposite said active surface, said protective layer shielding against

light and disturbing environmental influences.

23. The device according to Claim 22 wherein said protective layer comprises hardened polymeric material.

24. A semiconductor device comprising:

a semiconductor chip having a planar active surface including an integrated circuit, said surface having an inorganic protective overcoat and an organic protective overcoat, and said circuit having metallization patterns including a plurality of contact pads;

each of said contact pads having an added conductive layer on said metallization, said added layer having a conformal surface adjacent said chip, including peripheral portions of said overcoats, and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting.

25. The device according to Claim 24 wherein said organic overcoat is heat-resistant and compliant.

26. A semiconductor assembly comprising:

a semiconductor chip having a planar active surface including an integrated circuit protected by an inorganic overcoat, said circuit having metallization patterns including a plurality of contact pads, each of said contact pads having an added conductive layer on said metallization, said added layer having a conformal surface adjacent said chip and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting; and

an assembly board having a plurality of planar, metallurgically bondable terminal pads in a

distribution aligned with the distribution of said chip contact pads;

said chip metallurgically bonded to said board so that each of said chip contact pads is connected to a corresponding board terminal pad.

27. The assembly according to Claim 26 wherein said assembly board is selected from a group consisting of organic materials. Including FR-4, FR-5, and BT resin, with or without strengthening, thermally modulating fibers, or CTE-matching fillers; metals; and ceramics.

28. The assembly according to Claim 26 wherein said board terminal pads comprise an outer surface selected from a group consisting of gold, palladium, silver, platinum and alloys thereof.

29. The assembly according to Claim 26 wherein said metallurgical bonding of said outer layer surface of said contact pads to said terminal pads is selected from a group of techniques and materials comprising:

direct welding by metallic interdiffusion;

attachment by solder paste; and

attachment by conductive adhesive.

30. The assembly according to Claim 26 wherein said semiconductor chip has an additional organic protective overcoat over said inorganic overcoat.

31. The assembly according to Claim 26 wherein said semiconductor chip has a non-conductive adhesive layer over said overcoat, filling the spaces between said added conductive layers on each of said contact pads and further being attached to said assembly board.

32. A method for fabricating a semiconductor device comprising a semiconductor chip having a planar active surface including an integrated circuit protected by an inorganic overcoat, and a metallization pattern including a plurality of contact pads, comprising the step of:

depositing at least one added conductive layer on said metallization of said contact pads, said added layer having a conformal surface adjacent said chip and a portion of said overcoat, and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting.

33. The method according to Claim 32 wherein said step of depositing is selected from a group consisting of sputtering, evaporating, and plating.

34. The method according to Claim 32 wherein said step of fabricating a planar outer surface of said added layer comprises the step of depositing said at least one added conductive layer by electroless plating.

35. The method according to Claim 32 wherein said step of fabricating a planar outer surface of said added layer comprises the step of depositing said at least one added conductive layer by screen printing.

36. The method according to Claim 32 wherein said step of fabricating a planar outer surface of said added layer comprises the step of depositing said at least one added conductive layer as connecting bridges between support islands formed of protective overcoat.

37. A method for fabricating a semiconductor assembly comprising the steps of:

providing a semiconductor chip having a planar active surface including an integrated circuit protected

by an inorganic overcoat, and a metallization pattern including a plurality of contact pads, each of said contact pads having an added conductive layer on said metallization and a portion of said overcoat, said added layer having a conformal surface adjacent said chip and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting;

providing an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of said chip contact pads;

aligning said added chip metallization and said board pads so that each of said chip contact pads is connected to a corresponding board terminal pad; and

metallurgically bonding said chip metallization and said board pads.

38. The method according to Claim 37 wherein said bonding comprises one of the following assembly techniques:

- direct welding by metallic interdiffusion;
- attaching including solder paste;
- attaching including a conductive adhesive.